**What is claimed is:**

1. A M x N matrix display architecture comprising:

M x N display devices;

one video display controller and

one frame buffer,

wherein only the one frame buffer and the one video display controller are required to control timing and flow of image data to the M x N display devices.

2. The display architecture of claim 1 wherein the one video display controller comprises:

M line buffer systems for receiving image data from the frame buffer;

N line fetching systems associated with each line buffer system for fetching and processing image data from its associated line buffer system and

a data selector associated with each line buffer system for selecting the image data from one of the line fetching systems and sending the image data to one of the display devices.

3. The display architecture of claim 2 wherein each line buffer system comprises N line buffer segments storing image data to be sent to the line fetching systems.

4. The display architecture of claim 3 wherein each line fetching system comprises:

a memory interface receiving image data from the frame buffer;

a First-In-First-Out (FIFO) memory unit, and

a scaler unit for scaling image data received from the FIFO memory unit or image data received from the line buffer system.

5. The display architecture of claim 4 further comprising a Time Division Multiplex Image Display (TDMID) algorithm for determining which line fetching system the data selector sends image data from and for controlling the timing for sending the image data.

6. The display architecture of claim 1 wherein the video display controller comprises:

M line buffer systems;

N line fetching systems associated with each line buffer system;

N data selectors associated with each line buffer system, and

a Time Division Multiplex Image Display (TDMID) algorithm for controlling the timing and data flow of the video display controller.

7. The display architecture of claim 6 wherein each line buffer system comprises N line buffer segments storing image data to be sent to the line fetching systems.

8. The display architecture of claim 7 wherein each line fetching system comprises:

a memory interface receiving image data from the frame buffer;

a First-In-First-Out (FIFO) memory unit, and

a scaler unit for scaling image data received from the FIFO memory unit or image data received from the line buffer system.

9. The display architecture of claim 8 wherein the scaler unit comprises a horizontal scaler portion and a vertical scaler portion.

10. An M x N matrix display architecture comprising:

M x N display devices;

a frame buffer, and

a video display controller comprising

M line buffer systems for receiving image data from the frame buffer,

N line fetching systems associated with each line buffer system for fetching and processing image data from its associated line buffer system,

a data selector associated with each line buffer system for selecting the image data from one of the line fetching systems and sending the image data to one of the display devices and

a Time Division Multiplex Image Display (TDMID) algorithm for controlling the timing and operation of the data selector,

wherein only a single frame buffer and single video display controller combination are required to control timing and flow of image data to the M x N display devices.